UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/775,167	02/01/2001	Yasushi Kubota	55561 (820)	7275

21874 7590 07/30/2003

EDWARDS & ANGELL, LLP
P.O. BOX 9169
BOSTON, MA 02209

EXAMINER
NELSON, ALECIA DIANE

ART UNIT	PAPER NUMBER
2675	5

DATE MAILED: 07/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/775,167	KUBOTA ET AL.	
	Examiner	Art Unit	
	Alecia D. Nelson	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed within the application.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 02/01/01 was filed after has being considered by the examiner.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. ***Claims 1-11*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Maekawa (U.S. Patent No. 5,128,974) in view of Kawaguchi et al. (U.S. Patent No. 5,602,561).

With reference to **claims 1 and 5**, Maekawa teaches a shift register apparatus comprising unit registers, clocks, and gates (see abstract). The shift register (Fig. 7) is provided with a plurality of register blocks (SR1-SRn), which operates in synchronization with a clock signal and a transfer gate (SW1, SW2) for controlling the clock signal (VCLK, VCLK') supplied to the shift register, the plurality of register blocks being serially connected together (see column 4, lines 19-39, Fig. 7), and the transfer gate being brought into an ON-state every register block only in a specified period during which an output changes (see column 4, lines 49-60).

Maekawa fails to specifically teach that the shift register contains a flip-flop that operates in synchronization with a clock signal, or that the output of the flip-flop effects the state of the transfer gate. However as stated above Maekawa does teach that the shift register contains inverters (INV1-INV4), which have the claimed functionality of the flip-flop.

Kawaguchi et al. teaches a driving arrangement for a display apparatus wherein a shift register (11) which shifts a sampling signal in accordance with a clock signal (see

column 4, lines 39-43), and comprises D-type flip-flops (811) connected in series (see column 6, line 59-column 7, line 13).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the device of Maekawa to include the D-type flip flop operating in a manner similar to that which is taught by Kawaguchi et al. in order to thereby provide a shift register apparatus to be used in a liquid crystal display driver which consumes less power which reduces the drivers of clock signals.

With reference to **claim 2**, Maekawa teaches that when a level of an input signal inputted to each register block and a level of an output signal outputted from the register block differ from each other, the transfer gate of the register block is brought into the ON-state (see column 4, lines 49-60).

With reference to **claims 3 and 4**, Maekawa teaches that the register block has a logic operation section for executing a logic operation of an input signal of the register block and an output signal of the register block and controls the transfer gate to be turned on and off based on a signal representing a logic operation result of the operation section (see column 4, lines 32-39).

Maekawa fails to specifically teach the usage of a D-type flip-flop, however does teach the usage of inverters (INV1-INV4) which function as explained above.

Kawaguchi et al. teaches a driving arrangement for a display apparatus wherein a shift register (11) which shifts a sampling signal in accordance with a clock signal (see

column 4, lines 39-43), and comprises D-type flip-flops (811) connected in series (see column 6, line 59-column 7, line 13). With further reference to **claim 4**, neither reference specifically teaches the usage of an SR-type flip flop, however if it is obvious to use one type of flip-flop it would be obvious to use a different type of flip-flop as well.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the device of Maekawa to include the D-type flip flop operating in a manner similar to that which is taught by Kawaguchi et al. in order to thereby provide a shift register apparatus to be used in a liquid crystal display driver which consumes less power which reduces the drivers of clock signals.

With reference to **claims 6-11**, Maekawa teaches that the shift register is used in a liquid crystal display scanner to generate horizontal sampling pulses comprising a plurality of pixels arranged in a matrix form (3), a plurality of data signal lines for supplying image data to be written into the plurality of pixels, a plurality of scanning signal lines for controlling the image data to be written into the pixels, a data signal line drive circuit for driving the data signal lines and a scanning signal line drive circuit for driving the scanning signal lines (see column 1, line 50-column 2, line11). With further reference to **claims 9-11**, Maekawa fails to specifically teach that the data signal line and the scanning signal line drive circuits are formed on a substrate identical to that of the plurality of pixel, however, such an arrangement is well known in the art. As well as a polysilicon thin film transistor and the temperature range for forming the TFT on the glass substrate.

5. ***Claims 12-24*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Maekawa in view of Kawaguchi et al. as applied to claim 1 above, and further in view of Erhart et al. (U.S. Patent No. 5,572,211).

With reference to **claims 12-16**, Maekawa and Kawaguchi et al. fail to teach that the shift register circuit includes a level shifter for setting the clock signal to a lower level than the clock signal input level of the flip-flop

Erhart et al. teaches an integrated circuit for generating output voltages for a series of column driver output circuits used to drive a LCD display (see abstract). The column driver circuit includes a level shift block (166) wherein the clock signal is level-shifted to provide a level-shifted clocking signal which is coupled to the clock input terminals of each of the flip-flops of the shift register (158) (see column 10, lines 20-30). Further it is taught that that the circuitry allows for the voltages to be stepped in either direction, but is initially started at a low level which is applied to the input terminal of the first flip-flop (160) (see column 39-62). It is also taught that the Lower DAC (64) in which the shift register is contained receives several power supply voltages, including VSS1 (see column 8, lines 10-20).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the usage of the level shifter as taught by Erhar et al. in a system similar to that which is taught by Maekawa and Kawaguchi et al. to thereby provide an integrated circuit for an LCD wherein the shift register circuit is operated at a lower voltage, thereby allowing poser consumption to be further reduced.

With reference to **claims 17 and 18**, Maekawa teaches that the register block has a logic operation section for executing a logic operation of an input signal of the register block and an output signal of the register block and controls the trasfer gate to be turned on and off based on a signal representing a logic operation result of the operation section (see column 4, lines 32-39).

Maekawa fails to specifically teach the usage of a D-type flip-flop, however does teach the usage of inverters (INV1-INV4) which function as explained above.

Kawaguchi et al. teaches a driving arrangement for a display apparatus wherein a shift register (11) which shifts a sampling signal in accordance with a clock signal (see column 4, lines 39-43), and comprises D-type flip-flops (811) connected in series (see column 6, line 59-column 7, line 13). With further reference to **claim 18**, neither reference specifically teaches the usage of an SR-type flip flop, however if it is obvious to use one type of flip-flop it would be obvious to use a different type of flip-flop as well.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the device of Maekawa to include the D-type flip flop operating in a manner similar to that which is taught by Kawaguchi et al. in order to thereby provide a shift register apparatus to be used in a liquid crystal display driver which consumes less power which reduces the drivers of clock signals.

With reference to **claims 19-24**, Maekawa teaches that the shift register is used in a liquid crystal display scanner to generate horizontal sampling pulses comprising a

plurality of pixels arranged in a matrix form (3), a plurality of data signal lines for supplying image data to be written into the plurality of pixels, a plurality of scanning signal lines for controlling the image data to be written into the pixels, a data signal line drive circuit for driving the data signal lines and a scanning signal line drive circuit for driving the scanning signal lines (see column 1, line 50-column 2, line11). With further reference to **claims 22-24**, Maekawa fails to specifically teach that the data signal line and the scanning signal line drive circuits are formed on a substrate identical to that of the plurality of pixel, however, such an arrangement is well known in the art. As well as a polysilicon thin film transistor and the temperature range for forming the TFT on the glass substrate.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alecia D. Nelson whose telephone number is (703)305-0143. The examiner can normally be reached on Monday-Friday 9:30-7:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve Saras can be reached on (703)305-9720. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9314 for regular communications and (703)872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-9700.

adn/ADN
July 27, 2003

DENNIS-DOON CHOW
PRIMARY EXAMINER